

Circuit Applications of the AD2S90 Resolver-to-Digital Converter

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The AD2S90 is a 12-bit resolution monolithic resolver-to-digital converter. It provides a complete solution for digitizing resolver signals without using external components. The advantage of using the AD2S90 over other traditional R/D converters in the market is that this chip provides not only absolute position data output (in serial form), but also standard A Quad B format signals. When upgrading the incremental encoder system to a resolver based system, this chip plus a resolver will give out a complete replacement solution without revising the remainder of the system. The absolute position data output gives additional useful information in the upgraded system. The serial form of the digital position data is especially suitable for long distance data transmission.

This application note does not discuss the general features or the basic operations of the AD2S90; that information can be found in the data sheet. The following applications are discussed in this application note:

- Absolute position data serial-to-parallel conversion
- Absolute position data EIA-485 communication
- 4096 line incremental encoder emulation

ABSOLUTE POSITION DATA SERIAL-TO-PARALLEL CONVERSION

There are many different ways to perform AD2S90 absolute position data serial-to-parallel conversion. Proper digital timing can be generated using microprocessor or hardware circuits. The Figure 1 block diagram

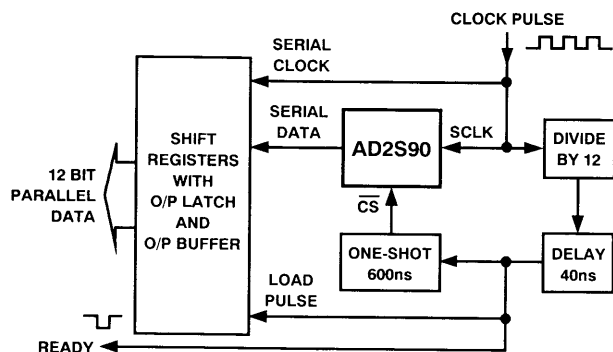
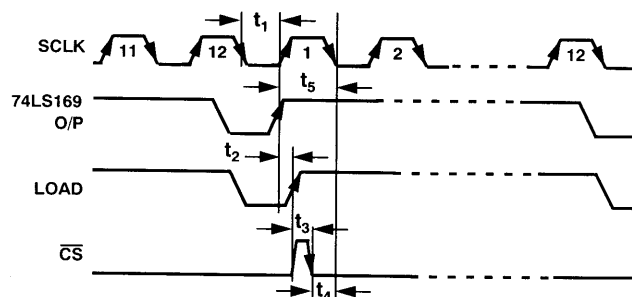


Figure 1. Serial-to-Parallel Conversion Block Diagram

demonstrates the basic AD2S90 serial-to-parallel data conversion in a hardware mode. In this scheme we use two 74HC595s as shift registers. The timing is generated by using a counter/divider 74LS169, 74121 monostable and a delay component. Figure 2 shows the implementation circuit in schematic form.

Considering the timing diagram of the device as shown in the data sheet, the clock pulse waveform (SCLK) should have the following relationships with the chip select pulse ($\overline{CS}$) and load pulse:



- Here, $t_1 = 250$ ns minimum
- $t_2 = 40$ ns (delay)
- $t_3 = 600$ ns minimum
- $t_4 = 600$ ns minimum

The value for t_5 can be easily calculated as:
 $t_5 = t_2 + t_3 + t_4 = 1240$ ns minimum.

In this application circuit, there is a maximum possible delay of 40 ns between the upgoing edge of SCLK and the upgoing edge of the 74LS169 output signal pulse. This has to be taken into consideration when calculating the timing.

The one-shot used in the Figure 2 circuit (74121) has the pulse width:

$$t_w = \ln 2 \cdot C \cdot R$$

with $C = 10$ pF and $R = 86.6$ k Ω , $t_w = 600$ ns

So the t_5 value in this circuit will be:

$$t_5 = t_2 + t_3 + t_4 + 40 = 1280$$
 ns minimum

The above 7-wire RS-485 data transmission configuration is basically designed for transmitting the AD2S90 serial data to a remote location where all the data is then converted to parallel. The block diagram of the whole system is shown in Figure 5.

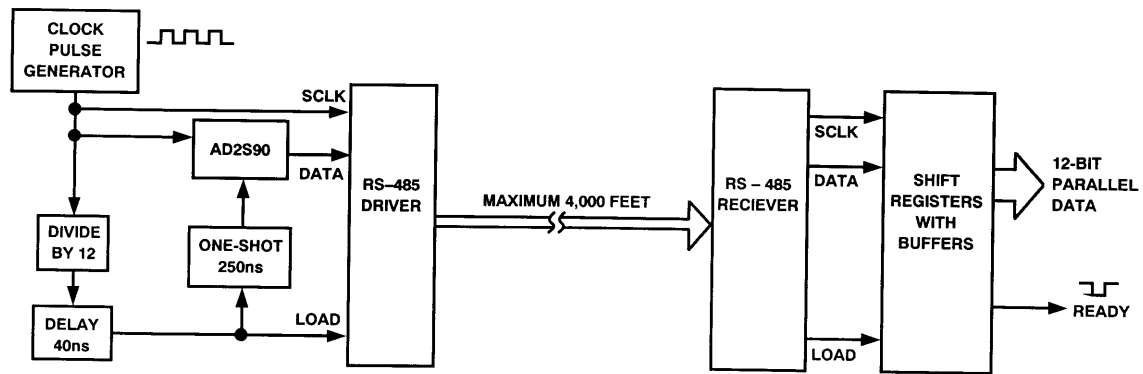


Figure 5. Serial-to-Parallel Data Transmission System Diagram

4096 LINE INCREMENTAL ENCODER EMULATION

One important feature that makes the AD2S90 unique among R/D converters is the quadrature signal output. The device gives out 1024 line A Quad B and north marker signals exactly emulating those from a 1024 line incremental optical encoder. The resolution of the A Quad B can be increased by multiplying the 1024 line count by 4. This produces a 4096 A Quad B output which can be decoded to 16384. An example of 4096 line incremental encoder emulation is shown in Figure 6. Cautions must be taken in selecting the inverter type shown in Figure 6. For example, 4000-Series CMOS will give you longer pulse durations than the AS logic family. In certain cases, inverters can be replaced by delay components to generate more precise timing.

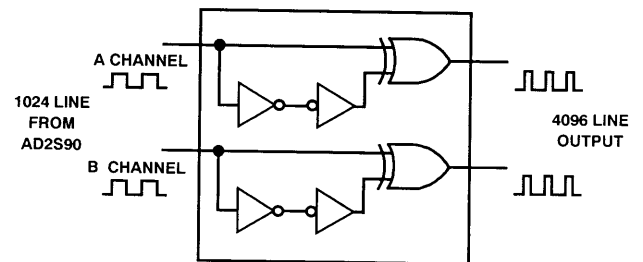


Figure 6. $\times 4$ Circuitry Offering 4096 Incremental Encoder Emulation Using the AD2S90